SSD1331 OLED Display Controller Interface Notes

Overview

- Pixel Dimensions: 96x64
- 16 bit color resolution
- Uses SPI to communicate from FPGA to PMOD
- Only write operations allowed in Serial mode

PMOD Pinout

- CS: Chip select, active high reset
- MOSI: Master out slave in
- SCK: serial clock
- D/C: Data/command control
 - If high, data is written to graphic display data RAM
 - If low, inputs at D0-D15 are interpreted as a command and will be decoded and written to corresponding command register
- RES: Power reset
- VCCEN: VCC Enable
- PMODEN: Vdd logic voltage control

Pin	Signal	Description
1	CS	Chip Select
2	MOSI	Master-Out-Slave-In
3	NC	Not Connected
4	SCK	Serial Clock
5	GND	Power Supply Ground
6	VCC	Power Supply (3.3V)
7	D/C	Data/Command Control
8	RES	Power Reset
9	VCCEN	Vcc Enable
10	PMODEN	Vdd Logic Voltage Control
11	GND	Power Supply Ground
12	VCC	Power Supply (3.3V)

PMOD Schematic



SPI Interface (Section 7.1.3, Page 17)

Function	E	R/W#	CS#	D/C#	
Write command	Tie low	Tie low	L	L	
Write data	Tie low	Tie low	L	Н	
Figure 8 - Write procedure in	SPI mode				
CS#				_	
D/C#				_	
SDIN/ SCLK	DB2	\propto	DBn		
/					
SCLK(D0)					
SDIN(D1)	06 D5	D4		D2	

Clock Timing

Table 21 - Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V, V_{DDIO} = 2.4V to V_{DD}, T_A = 25°C)

Symbol	Parameter	Min	Тур	Max	Unit
t _{cycle}	Clock Cycle Time	150	-	-	ns
tas	Address Setup Time	40	-	-	ns
tan	Address Hold Time	40	-	-	ns
t _{css}	Chip Select Setup Time	75	-	-	ns
t _{csH}	Chip Select Hold Time	60	-	-	ns
t _{osw}	Write Data Setup Time	40	-	-	ns
t _{orrw}	Write Data Hold Time	40	-	-	ns
tolkl	Clock Low Time	75	-	-	ns
t _{CLKH}	Clock High Time	75	-	-	ns
t _R	Rise Time	-	-	15	ns
tF	Fall Time	-	-	15	ns





Minimum SCLK cycle time = 150ns

- Maximum 6.66 MHz
- With 100MHz clock, can use divider 100 for 1 MHz clock

Reset Circuit

When RES pulled low, chip is initialized with the following:

- 1. Display is OFF
- 2. 64 MUX display mode
- 3. Display start line is set at display RAM address 0
- 4. Display offset set to 0
- 5. Normal segment and display data column address and row address mapping
- 6. Column address counter is set at 0
- 7. Master contrast control register is set at OFH
- 8. Individual contrast control registers of color A, B, and C are set to 80H
- 9. Shift register data clear in serial interface
- 10. Normal display mode (equivalent to A4 command)

Power on sequence

Bytes provided are in format of (command, data)

- 1. Bring D/C control to logic low
- 2. Bring the reset pin logic high
- 3. Bring the VCC Enable logic low
- 4. Bring PMODEN to high, wait 20 ms
- 5. Bring RES logic low, wait at least 3 us, then bring back to logic high to reset display controller
- 6. Wait for reset to complete, max of 3 us
- 7. Enable driver IC to accept command by sending unlock command over SPI (0xFD, 0x12)
- 8. Send display off command (0xAE)

Power on from SSD1331 Datasheet:

- 1. Power ON VDD, VDDIO
- 2. After VDD stable, set RES pin LOW for atleast 3us, and then HIGH
- 3. Wait atleast 3 uS to power on VCC
- 4. After VCC is stable, send command 0xAF to power display ON, will be on after 100ms



Figure 19 : The Power ON sequence

Power off sequence

- 1. Turn the display off (0xAE)
- 2. Bring VCCEN low
- 3. Delay 400 ms
- 4. Power off VDD



Graphic Display Data RAM (GDDRAM)

- Bit mapped static RAM holding pattern to be displayed
- RAM size is 96x64x16 bits
- Each pixel has 16-bit data
- Three sub pixels for color A, B, and C have 5 bits, 6 bits, and 5 bits respectively

Column	Normal		0			1			2		1		93			94			95		
Address	Remap		95			94			93		11		2			1			0		
Da	ata	A4	B5	C4	A4	B5	C4	A4	B5	C4		A4	B5	C4	A4	B5	C4	A4	B5	C4	
For	mat	A3	B4	C3	A3	B4	C3	A3	B4	C3		A3	B4	C3	A3	B4	C3	A3	B4	C3	
		A2	B3	C2	A2	B3	C2	A2	B3	C2		A2	B 3	C2	A2	B3	C2	A2	B3	C2	
	\mathbf{N}	A1	B2	C1	A1	B2	C1	A1	B2	C1		A1	B2	C1	A1	B2	C1	A1	B2	C1	
Add	ow trocc	A0	B1	C0	A0	B1	C0	A0	B1	C0		A0	B1	C0	A0	B1	C0	A0	B1	C0	
Auu	liess		BO			BO			BO				BO			BO			B0		COM
Normal	Remap																				OUTPUT
0	63	5,	6	5	5	6	5	5	6	5		5	6	5	5	6	5	5	6	5	COM0
1	62	-	<								1										COM1
2	61		\backslash																		COM2
:	:			no. c	of bit	s of	data	in th	nis ce	ell											:
61	2																				COM61
62	1										1										COM62
63	0																				COM63
SEG O		SAO	SB0	SCO	SA1	SB1	SC1	SA2	SB2	SC2		SV03	\$803	SC93	SA04	SR04	9004	SA05	SR05	SC05	

Figure 10 - 65k Color Depth Graphic Display Data RAM Structure

- Can also choose different color depth to save on transmit size

Table 9 - Data bus usage under different bus width and color depth mode

			Data	bus											_			
Bus width	Color Depth	Input order	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8 bits	256		х	х	х	Х	х	х	Х	Х	C4	C ₃	C ₂	B ₅	B4	B ₃	A4	A ₃
8 bits	65k format 1	lst	х	х	х	х	х	х	х	х	C4	C ₃	C ₂	Cı	C ₀	B ₅	B4	B ₃
		2nd	х	х	х	х	х	х	х	х	B ₂	B	B ₀	- A ₄	A ₃	A ₂	A	\mathbf{A}_{0}
8 bits	65k format 2	1st	x	x	x	х	х	х	х	x	х	х	C ₄	C ₃	C ₂	C	C ₀	х
		2nd	х	х	х	Х	х	х	х	х	х	х	B 5	B ₄	B ₃	B ₂	Bi	B ₀
		3rd	х	х	х	х	х	х	х	х	х	х	A4	A ₃	A ₂	A ₁	A ₀	х
16 bits	65k		C4	C ₃	C ₂	C	C ₀	B 5	B ₄	B ₃	B ₂	Bi	B ₀	A4	A ₃	A ₂	A	A ₀
9 bits	65k	1st	Х	х	X	Х	х	х	Х	C ₄	C ₃	C ₂	Ci	C ₀	Х	B 5	B ₄	B ₃
		2nd	х	х	х	Х	х	х	х	B ₂	Bi	B ₀	A4	A ₃	A ₂	A	A ₀	х

At 65k color depth mode, color A, B, C are directly mapped to the RAM content. At 256-color mode, the RAM content will be filled up to 65k format.

Figure	11	- 256-color	mode	map	ping
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_				SCn					S	3n					SAn		
I	65k color	C ₄	C ₃	C2	C ₁	C ₀	B ₅	B ₄	B ₃	B ₂	\mathbf{B}_1	B ₀	A4	A3	A ₂	A	A ₀
[256 color	C4	C3	C2	*C4	*C4	B ₅	B ₄	B ₃	B ₅	*B5	*B5	A ₄	A ₃	*A4	*A4	*A4

Note: ⁽¹⁾ n = 0 ~ 95 ⁽²⁾ bits with * are copied from corresponding bits in order to fill up 65K format.

Remap and Color Depth Setting

Fund	lamenta	I Co	mm	and	s							
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	Default
0	A0	1	0	1	0	0	0	0	0		Set driver remap and color depth	
0	A[7:0]	A7	A ₆	A_5	A_4	A ₃	A ₂	A ₁	A ₀		A[0]=0, Horizontal address increment	A[0]=0
											A[0]=1, Vertical address increment	
											A[1]=0, RAM Column 0 to 95 maps to Pin Seg (SA,SB,SC) 0 to 95 A[1]=1, RAM Column 0 to 95 maps to Pin Seg (SA,SB,SC) 95 to 0	A[1]=0
											A[2]=0, normal order SA.SB.SC (e.g. RGB)	A[2]=0
											A[2]=1, reverse order SC,SB,SA (e.g. BGR)	
										Remap & Color	A[3]=0, Disable left-right swapping on COM A[3]=1, Set left-right swapping on COM	A[3]=0
										Depth setting	A[4]=0, Scan from COM 0 to COM [N -1]	A[4]=0
											A[4]=1, Scan from COM [N-1] to COM0. Where N is the multiplex ratio.	
											A[5]=0, Disable COM Split Odd Even (RESET)	A[5]=0
											A[5]=1, Enable COM Split Odd Even	
											A[7:6] = 00; 256 color format	
											A[7:6] = 01; 65k color format	A[7:6]=01
											A[7:6] = 10; 65k color format 2	
											If 9 / 18 bit mode is selected, color depth will be fixed to 65k regardless of the setting.	

This command has multiple configurations and each bit setting is described as follows.

Address increment mode (A[0])

When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 23.

	Col 0	Col 1		Col 94	Col 95
Row 0					1
Row 1	t				ţ
:	4:		:		
Row 62					ţ
Row 63					

Figure 23 - Address Pointer Movement of Horizontal Address Increment Mode

When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 24.

Figure 24 - Address Pointer Movement of Vertical Address Increment Mode

	Co	0 10	Co	11		Co	94	Col	95
Row 0									1
Row 1					/				
					: /				
Row 62					/				
Row 63		1		1			1		,

Set Display Mode

Fund	amenta	l Co	mm	and	s							
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	Default
0	A4 /	1	0	1	0	0	1	X_1	X ₀		A4h=Normal Display	A4h
0	A5 /									Set Display	A5h=Entire Display ON, all pixels turn ON at GS63	
0	A6 /									Mode	A6h=Entire Display OFF, all pixels turn OFF	
0	A7 /										A7h=Inverse Display	

Set Display ON/OFF (0xAD)

0	AC AE AF	1	0	1	0	1	1	A ₁	A	Set Display ON/OFF	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) AFh = Display ON in normal mode	AEh
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Display Functions

- Pages 28 through 33 of datasheet
- Additional functions on page 35

Drawing a Line

Create a line between two sets of points with the command 0x21

- 1. Enter into draw line mode with command 0x21
- 2. Send column start address of line, column1, for example 0x01
- 3. Send row start address of line, row1, for example 0x10
- 4. Send column end address of line, column 2, for example 0x28
- 5. Send row end address of line, row 2, for example 0x04
- 6. Send color C, B, and A of line, for example 35d, 0d, 0d for blue color



Drawing a rectangle

Create a rectangle with a specific command 0x22

- 1. Enter "Draw rectangle mode" by execute command 0x22
- 2. Set starting column coordinates, column 1, for example 0x03
- 3. Set starting row coordinates, Row 1, for example 0x02
- 4. Set finishing column coordinates, column 2, for example 0x12
- 5. Set finishing row coordinates, Row 2, for example 0x15
- 6. Set outline color C, B, and A, for example 28, 0, and 0 for blue color
- 7. Set filled color C, B, and A, for example 0, 0, and 40 for red color



Сору

Copy the rectangular region defined by starting point (row 1, col 1) and the ending point (row 2, col 2) to location (row 3, col 3). If new coordinates are smaller than the ending points, the new image will overlap with original one.

- 1. Enter copy mode with command 0x23
- 2. Set starting column coordinates, Column 1, for example 0x00
- 3. Set starting row coordinates, row 1, for example 0x00
- 4. Set finishing column coordinates, Column 2, for example 0x055
- 5. Set finishing row coordinates, row 2, for example 0x05
- 6. Set new column coordinates, column 3, for example 0x03
- 7. Set new row coordinates, row 3, for example 0x03



Dim Window

Command will dim window area specify by starting point (row 1, col 1) and the ending point (row 2, col 2). After execution of this command, the selected window area will become darker as follows:

Original gray scale	New gray scale after dim window command
GS0 ~ GS15	No change
GS16 ~ GS19	GS4
GS20 ~ GS23	GS5
:	:
GS60 ~ GS63	GS15

Table 15 - Result of Change of Brightness by Dim Window Command

Additional execution of this command over the same window area will not change the data content

Clear Window

This command sets the window area specify by starting point (row 1, col 1) and the ending point (row 2, col 2) to clear the window display. The graphic display data RAM content of the specified window will be set to 0

- 1. Set clear mode with command 0x25
- 2. Set starting col 1
- 3. Set starting row 1
- 4. Set finish col 2
- 5. Set finish row 2



Fill Enable/Disable

This command has two functions:

- 1. Enable/Disable fill (A[0])
 - a. 0: disable filling of color into rectangle in draw rectangle command (RESET)
 - b. 1: enable filling of color into rectangle in draw rectangle command
- 2. Enable/Disable reverse copy(A[4])
 - a. 0: Disable reverse copy (RESET)
 - b. 1: during copy command, the new image colors are swapped

Scrolling

Setup command is 0x27



Should not change setup parameters after scrolling has been activated (deactivate first!)

Deactivate scrolling: 0x2E

Activate scrolling: 0x2F